## Example: Interpretation of a Digital Circuit

Here is a sample problem, taken from the textbook The Essentials of Computer Organization and Architecture by Linda Null and Julia Lobur.


The task is to represent this circuit by both a Boolean expression and a Truth Table. Admittedly, this will prove to be a silly circuit.

## Interpreting a Digital Circuit: Step 1

Label the circuit elements (I have chosen to use numbers) and label the output of each element. Note that we are slowly building a Boolean expression.


The outputs of each gate are as follows:
The output of gate 1 is $(\mathrm{X}+\mathrm{Y})$,
The output of gate 2 is $(\mathrm{Y} \oplus \mathrm{Z})$,
The output of gate 3 is $X^{\prime}$,
The output of gate 4 is $\mathrm{X}^{\prime}+(\mathrm{Y} \oplus \mathrm{Z})$, and
The output of gate 5 is $(\mathrm{X}+\mathrm{Y}) \oplus\left[\mathrm{X}^{\prime}+(\mathrm{Y} \oplus \mathrm{Z})\right]$

## Interpreting a Digital Circuit: Step 2

For a circuit of this complexity, the best next step is to make a Truth Table.

| X | Y | Z | $\mathbf{X}+\mathbf{Y}$ | $(\mathrm{Y} \oplus \mathrm{Z})$ | $\mathrm{X}^{\prime}$ | $\mathrm{X}^{\prime}+(\mathbf{Y} \oplus \mathbf{Z})$ | $(\mathrm{X}+\mathrm{Y}) \oplus\left[\mathrm{X}^{\prime}+(\mathrm{Y} \oplus \mathrm{Z})\right]$ |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| 0 | 0 | 0 | $\mathbf{0}$ | 0 | 1 | $\mathbf{1}$ | 1 |
| 0 | 0 | 1 | $\mathbf{0}$ | 1 | 1 | $\mathbf{1}$ | 1 |
| 0 | 1 | 0 | $\mathbf{1}$ | 1 | 1 | $\mathbf{1}$ | 0 |
| 0 | 1 | 1 | $\mathbf{1}$ | 0 | 1 | $\mathbf{1}$ | 0 |
| 1 | 0 | 0 | $\mathbf{1}$ | 0 | 0 | $\mathbf{0}$ | 1 |
| 1 | 0 | 1 | $\mathbf{1}$ | 1 | 0 | $\mathbf{1}$ | 0 |
| 1 | 1 | 0 | $\mathbf{1}$ | 1 | 0 | $\mathbf{1}$ | 0 |
| 1 | 1 | 1 | $\mathbf{1}$ | 0 | 0 | $\mathbf{0}$ | 1 |

We have now solved the problem. I want to continue and produce a simpler expression. (At least I think that it is simpler).

## Interpreting a Digital Circuit: Step 3

Present the truth table without the intermediate expressions. Use the standard rules to convert the truth table to either Canonical SOP or Canonical POS.
We do both.

| X | Y | Z | $\mathrm{F}(\mathrm{X}, \mathrm{Y}, \mathrm{Z})$ |
| :---: | :---: | :---: | :---: |
| 0 | 0 | 0 | 1 |
| 0 | 0 | 1 | 1 |
| 0 | 1 | 0 | 0 |
| 0 | 1 | 1 | 0 |
| 1 | 0 | 0 | 1 |
| 1 | 0 | 1 | 0 |
| 1 | 1 | 0 | 0 |
| 1 | 1 | 1 | 1 |

SOP: $\quad \mathrm{F}(\mathrm{X}, \mathrm{Y}, \mathrm{Z})=\mathrm{X}^{\prime} \cdot \mathrm{Y}^{\prime} \cdot \mathrm{Z}^{\prime}+\mathrm{X}^{\prime} \cdot \mathrm{Y}^{\prime} \cdot \mathrm{Z}^{\mathrm{Z}}+\mathrm{X} \bullet \mathrm{Y}^{\prime} \cdot \mathrm{Z}^{\prime}+\mathrm{X} \bullet \mathrm{Y} \bullet \mathrm{Z}$

$$
000 \quad 001 \quad 100 \quad 111
$$

POS: $\mathrm{F}(\mathrm{X}, \mathrm{Y}, \mathrm{Z})=\left(\mathrm{X}+\mathrm{Y}^{\prime}+\mathrm{Z}\right) \bullet\left(\mathrm{X}+\mathrm{Y}^{\prime}+\mathrm{Z}^{\prime}\right) \bullet\left(\mathrm{X}^{\prime}+\mathrm{Y}+\mathrm{Z}^{\prime}\right) \bullet\left(\mathrm{X}^{\prime}+\mathrm{Y}^{\prime}+\mathrm{Z}\right)$

## Interpreting a Digital Circuit: Step 4

SOP:

$$
\begin{aligned}
\mathrm{F}(\mathrm{X}, \mathrm{Y}, \mathrm{Z}) & =\mathrm{X}^{\prime} \bullet \mathrm{Y}^{\prime} \bullet \mathrm{Z}^{\prime}+\mathrm{X}^{\prime} \bullet \mathrm{Y}^{\prime} \bullet \mathrm{Z}+\mathrm{X}^{\prime} \bullet \mathrm{Y}^{\prime} \bullet \mathrm{Z}^{\prime}+\mathrm{X} \bullet \mathrm{Y}^{\prime} \bullet \mathrm{Z}^{\prime}+\mathrm{X} \bullet \mathrm{Y} \bullet \mathrm{Z} \\
& =\mathrm{X}^{\prime} \bullet \mathrm{Y}^{\prime} \bullet\left(\mathrm{Z}^{\prime}+\mathrm{Z}\right)+\left(\mathrm{X}+\mathrm{X}^{\prime}\right) \bullet \mathrm{Y}^{\prime} \bullet \mathrm{Z}^{\prime}+\mathrm{X} \bullet \mathrm{Y} \bullet Z \\
& =\mathrm{X}^{\prime} \bullet \mathrm{Y}^{\prime}+\mathrm{Y}^{\prime} \bullet \mathrm{Z}^{\prime}+\mathrm{X} \bullet \mathrm{Y} \cdot \mathrm{Z}
\end{aligned}
$$

POS:

$$
\begin{aligned}
\mathrm{F}(\mathrm{X}, \mathrm{Y}, \mathrm{Z}) & =\left(\mathrm{X}+\mathrm{Y}^{\prime}+\mathrm{Z}\right) \bullet\left(\mathrm{X}+\mathrm{Y}^{\prime}+\mathrm{Z}^{\prime}\right) \bullet\left(\mathrm{X}^{\prime}+\mathrm{Y}+\mathrm{Z}^{\prime}\right) \\
& \bullet\left(\mathrm{X}^{\prime}+\mathrm{Y}^{\prime}+\mathrm{Z}\right) \bullet\left(\mathrm{X}+\mathrm{Y}^{\prime}+\mathrm{Z}\right) \\
& =\left(\mathrm{X}+\mathrm{Y}^{\prime}\right) \bullet\left(\mathrm{X}^{\prime}+\mathrm{Y}+\mathrm{Z}^{\prime}\right) \bullet\left(\mathrm{Y}^{\prime}+\mathrm{Z}\right)
\end{aligned}
$$

One can also write

$$
\begin{aligned}
& \mathrm{F}(\mathrm{X}, \mathrm{Y}, \mathrm{Z})=\Sigma(0,1,4,7) \\
& \mathrm{F}(\mathrm{X}, \mathrm{Y}, \mathrm{Z})=\Pi(2,3,5,6)
\end{aligned}
$$

This is about as simple as I can make these expressions.

## Building a Digital Circuit for a Boolean Expression

We take as examples two representations of the same Boolean expression.

$$
\begin{aligned}
& F 2(A, B, C)=(\bar{A} \cdot B \cdot C)+(A \cdot \bar{B} \cdot C)+(A \cdot B \cdot \bar{C})+(A \cdot B \cdot C) \\
& G 2(A, B, C)=(A+B+C) \bullet(A+B+\bar{C}) \cdot(A+\bar{B}+C) \bullet(\bar{A}+B+C)
\end{aligned}
$$

Sum of Products
SOP One OR gate connecting the output of a number of AND gates.

$$
F 2(A, B, C)=(\bar{A} \cdot B \cdot C)+(A \cdot \bar{B} \cdot C)+(A \cdot B \cdot \bar{C})+(A \cdot B \cdot C)
$$



## Building a Digital Circuit (Part 2)

$$
\begin{aligned}
& F 2(A, B, C)=(\bar{A} \cdot B \cdot C)+(A \cdot \bar{B} \cdot C)+(A \cdot B \cdot \bar{C})+(A \cdot B \cdot C) \\
& G 2(A, B, C)=(A+B+C) \bullet(A+B+\bar{C}) \cdot(A+\bar{B}+C) \bullet(\bar{A}+B+C)
\end{aligned}
$$

## Product of Sums

POS One AND gate connecting the output of a number of OR gates.

$$
G 2(A, B, C)=(A+B+C) \cdot(A+B+\bar{C}) \cdot(A+\bar{B}+C) \cdot(\bar{A}+B+C)
$$



There are simpler Boolean expressions that are equivalent to both F2 and G2, which are equivalent to each other. We study simplification later.

## Stylistics

There are very few issues involved in drawing a digital implementation of a Boolean circuit. The basic issue is DRAWING NEATLY.

My style of having the inputs at the top, with each input immediately feeding a NOT gate, if necessary, is only a convention. It helps me minimize the clutter in a drawing. The student may adopt any style that is easy to understand.

## Big Gates

This style will ask for gates with a large number of inputs. Here is an 8-input AND fabricated from three 4-input AND gates.


The AND gate on the right could also be a 2-input or 3-input gate.

